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REMARKS

Claims 15-34, all the claims pending in the application, stand rejected only on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 15-18, 21-24, and 27-32 stand rejected under 35 U.S.C. §103(a) as being anticipated by Filipiak (U.S. Patent No. 5,447,887), hereinafter "Filipiak," and claims 19-20, 25-26, and 33-34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Filipiak in view of Dass et al. (U.S. Patent 6,046,101) hereinafter "Dass." Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Filipiak

1. The Position in the Office Action

Regarding claims 15-16, the Office Action states that Filipiak discloses a semiconductor device comprising (Fig. 5) a first level (30) of silicide free copper; and an uppermost layer (32) of copper, wherein a top of the uppermost layer comprises a silicide surface. However, the Office Action notes that Filipiak does not explicitly teach that the copper layer is a bonding pad. The Office Action further states that the copper layer may act as the bonding pad in the integrated circuit device. The Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the copper interconnect layer as a bonding pad in an IC device in order to provide electrical connect to a solder bump.

The Office Action asserts that, in claim 17, Filipiak discloses substantially the entire claimed structure, as applied to claim 15 above, except the method of cleaning of the uppermost

layer by applying one of the ammonia plasma and the hydrogen plasma. The Office Action declares that this is a product-by-process limitation. The Office Action proposes that, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself and that the patentability of a product does not depend on its method of production.

The Office Action further declares that if the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. The Office Action cites *In re Thorpe*, 777 F.2d 695, 698 USPQ 964, 966 (Fed. Cir. 1985). The Office Action also cites MPEP 2113. Moreover, the Office Action declares that an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" or not.

Regarding claim 18, the Office Action recites that Filipiak discloses all of the claimed structure, as applied to claim 15 above, except the silicide thickness, which is in the range of 10% to 20% of the total thickness of the copper interconnect layer. However, the Office Action discloses that Filipiak mentions the thickness of silicide can be changed, depending on the application of the device. The Office Action refers to Col. 5, line 63 - Col. 6, line 6. The Office Action then concludes that it would have been obvious to one skilled in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that, where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Regarding claims 21-23, 27-31, the Office Action states that Filipiak discloses a semiconductor device comprising (Fig. 5) an exterior surface having a silicide layer; and an interior having a copper layer, wherein the silicide layer comprises a bonding pad. Filipiak does not teach the thickness which is in the range 10 % to 20 % of the total thickness of the copper interconnect layer. However, the Office Action asserts that Filipiak mentions that the thickness of silicide can be changed depending of the application of the device. The Office Action cites Col.5, line 63 - Col. 6, line 6. The Office Action, thus, concludes that it would have been

obvious in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that, where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Regarding claims 24 and 32, the Office Action states that Filipiak discloses all of the claimed structure except the method of cleaning an uppermost layer by applying one of the ammonia plasma and the hydrogen plasma. Further, the Office Action declares that this is a product-by-process limitation and, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The Office Action concludes that the patentability of a product does not depend on its method of production. Also, the Office Action asserts that, if the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable, even though the prior product was made by a different process. The Office Action cites *In re Thorpe*, 777 F. 2d 695, 698 USPQ 964, 966 (Fed. Cir. 1985). The Office Action also cites MPEP 2113. Moreover, the Office Action declares that an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process".

2. The Filipiak Reference

Filipiak discloses that a silicon nitride layer (34) has improved adhesion to underlying copper interconnect members (30) through the incorporation of an intervening copper silicide layer (32). Layer (32) is formed in-situ with a plasma enhanced chemical vapor deposition (PECVD) process for depositing a silicon nitride layer (34). To form layer (32), a semiconductor substrate (12) is provided having a desired copper pattern formed thereon. The copper pattern may include copper interconnects, copper plugs, or other copper members. The substrate is placed into a PECVD reaction chamber. Silane is introduced into the reaction chamber in the absence of a plasma to form a copper silicide layer on any exposed copper surfaces. After a silicide layer of a sufficient thickness (for example, 10 to 100 angstroms) is formed, PECVD

silicon nitride is deposited. The copper silicide layer improves adhesion such that the silicon nitride layer is less prone to peeling away from underlying copper members.

3. Applicants' Response

In response to Applicants' previous arguments, the Office Action argues that Filipiak teaches that it would be appropriate to silicide the entire thickness of the copper member (col. 6, lines 5-6) and that it would have been obvious to select the thickness defined in the claims as merely an optimum or workable range involving only routine skill in the art. However, such reasoning ignores that the invention maintains performance of the semiconductor device irrespective of resistivity shifts. To the contrary, silicide in the entire thickness of the copper member would cause significant resistivity problems (as explained in Filipiak).

Indeed, the teachings in col. 6, lines 1-13, of Filipiak explain that the salicide should consume much less than 10% (and preferably 2%) of the metalization layer in order to avoid resistivity problems. The claimed invention is substantially different in that it forms the silicide to a thickness of 10-20% without altering performance (irrespective of resistivity shifts). More specifically, independent claims 15, 21, and 29 define that the upper layer "maintains performance of said semiconductor device irrespective of resistivity shifts." Therefore, since Filipiak teaches that anything above 10% silicide will have an unacceptable resistivity shift, Filipiak teaches away from the claimed invention and independent claims 15, 21, and 29 are not, and cannot be, taught or suggested by Filipiak.

An important feature of the invention is that it reduces such delamination by forming the silicide layer over the last metalization layer to, generally, at least 10-20% of the thickness of the LM layer. As pointed out in Filipiak, the silicide layer should not exceed 10% of the thickness of the underlying copper metal layer because silicide thicknesses in excess of 10% cause excessive resistance. However, the inventors discovered that this extensive silicide formation is acceptable at the last metal level to resolve the copper/nitrite adhesion issues, primarily because the last

metalization layer generally comprises very thick metallurgy and is, therefore, substantially less sensitive to resistivity shifts. Thus, with the claimed invention, the resistivity problems noted with conventional copper silicide (CuSi) systems is avoided. In other words, even though the invention forms the silicide layer thicker than the 10% limit which is known conventionally, the resistance problems are avoided because the last metalization layer 11 is substantially thicker than the metalization layers below in the underlying structure.

Filipiak states that where resistivity is not as important, the silicide thickness may not need to be as tightly controlled (col. 6, lines 1-4). This sentence makes no suggestion as to where or when the silicide thickness may exceed 10%. Most certainly, Filipiak does not suggest that the last metalization layer (bonding pad) has an excessively thick silicide layer that does maintain performance irrespective of resistivity shifts, as in the claimed invention. Further, the wording of the sentence "silicidation thickness may not need to be as tightly controlled" only insinuates that the thickness may deviate a very small amount from the 10% limit. For example, such language insinuates that possibly a fraction of a percent deviation might be acceptable. Such language clearly does not contemplate doubling the size of the silicide layer as in the claimed invention. Therefore, this sentence in Filipiak does not teach or suggest the inventive concept of doubling the thickness of the silicide layer of only the last metalization layer (bonding pad) in order to address adhesion issues. Thus, Applicants respectfully submit that Filipiak does not teach or suggest the 10% to 20% silicided surface defined by dependent claim 18 and independent claims 21 and 29.

Further, the Office Action admits that Filipiak does not disclose siliciding the last metalization layer 4 (the bonding pad). Instead, the Office Action merely concludes (without any additional support) that the copper layer disclosed in Filipiak "may act as the bonding pad in the integrated circuit device." However, such a statement is pure conjecture and is not based upon any teaching in the prior art of record. Indeed, such reasoning appears to be based upon hindsight because the Office Action implies such a modification of the reference, without any teaching showing why such modification would be made.

Therefore, as discussed above, an important feature of the claimed invention is that the top surface of the last metalization layer (bonding pad) is silicided (line 15) and that the silicided portion of the last metalization layer is in the range of approximately 10% to 20% (claims 18, 21, and 29). Applicants have previously argued that prior art teachings require that the silicide portion not exceed 10%; otherwise, excessive resistance would occur. This argument is supported by the language relied upon in the Office Action (column 5, lines 63-column 6, line 1 in Filipiak). Therefore, it is Applicants' position that the last metalization layer having a silicide layer thicker than 10%, in order to prevent delamination, is a novel structure. Further, the inventive structure breaks away from conventional teachings because the excessively thick silicide layer does not result in excessive resistance, as discussed above. Therefore, Applicants respectfully submit that independent claims 15, 21, and 29 are patentable over Filipiak. Further, dependent claims 16-18, 22-24, 27, 28, and 30-32 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Filipiak in view of Dass

1. The Position in the Office Action

With regard to claims 19-20, 25-26, and 33-34, the Office Action states that Filipiak teaches all claimed structure, as applied to claims 15, 21, & 29 above, except the tin solder terminal electrically connected to the bonding pad. However, the Office Action asserts that Dass teaches in Fig. 21 the solder terminal (270) connected to the bonding pad and a silicon nitride (245) including an opening. The Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder terminal in order

to facilitate an electrical connection of the semiconductor structure with an external connector, such as a modulator package substrate.

2. The Dass Reference

Dass discloses an integrated circuit passivation layer including a first passivation layer portion of silicon nitride treated with nitrous oxide and a second passivation layer portion of polymide. Also, a method of passivating an integrated circuit wafer including depositing a first passivation layer over the top surface of an integrated circuit wafer having a scribe street area between adjacent integrated circuit device portions, depositing a second passivation layer over the first passivation layer, and patterning the first passivation layer and the second passivation layer to expose the scribe street area.

3. Applicants' Response

The Dass reference is only utilized in the Office Action to show the use of tin solder when connecting to a bonding pad. Dass is silent regarding siliciding the upper layer of the bonding pad. Therefore, Dass does not cure the deficiencies of Filipiak as discussed above. Thus, even if one ordinarily skilled in the art had combined Dass and Filipiak, the proposed combination would not teach or suggest the invention as defined by independent claims 15, 21, and 29, as discussed above. Therefore, these independent claims are patentable over the proposed combination of references. Further, dependent claims 19-20, 25-26, and 33-34 are similarly patentable thought, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, Applicants respectfully request that the Examiner reconsider and withdraw this rejection.

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II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 15-34, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies in fees and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 12/17/01

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Attachment

Marked up Version of Changes Made

15. (Amended) A semiconductor device having at least two levels of interconnecting metallurgy, said semiconductor device comprising:

a first level of substantially silicide free metallurgy; and

an uppermost layer of metallurgy including a bonding pad, wherein a top of said uppermost layer comprises a silicided surface,

wherein said uppermost layer maintains performance of said semiconductor device irrespective of resistivity shifts.

21. (Amended) A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

wherein said silicided surface maintains performance of said semiconductor device irrespective of resistivity shifts.

29. (Amended) A semiconductor chip comprising:

an exterior surface having a top level of metallurgy; and

an interior having at least one internal level of metallurgy,

wherein said top level of metallurgy is thicker than said internal level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface,

wherein said silicided surface maintains performance of said semiconductor device irrespective of resistivity shifts.